8-13-03 #16

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Application No.: 09/399,281
Filed: September 17, 1999
Inventor(s):
James B. Keller and Derrick R. Meyer

Title: Virtual Channels and Corresponding Buffer Allocations for Deadlock-Free Computer System Operation

Examiner: Jean, Frantz B.
Group/Art Unit: 2155
Atty. Dkt. No: 5500-46300

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Lawrence J. Merkel
Printed Name

Signature 12/18/02
Date

# APPEAL BRIEF

Assistant Commissioner for Patents
Washington, D.C. 20231

Dear Sir:

Further to the Notice of Appeal filed November 15, 2002, Appellants present this Appeal Brief.



## I. REAL PARTY IN INTEREST

The Real Party in Interest in the present appeal is Advanced Micro Devices, Inc., the assignee. An assignment document has been executed by the inventors, but the Notice of Recordation has not yet been received by the assignee.

## II. RELATED APPEALS AND INTERFERENCES

There are no related appeals or interferences known to Appellants, Appellants legal representatives or assignee which will directly affect, be directly affected by, or have a bearing on the Board's decision in the pending appeal.

## III. STATUS OF CLAIMS

Claims 1, 3-9, and 12-29 are pending in the present application. Claims 1, 3-4, 6-

10, 13, 20-22, and 29 were rejected under 35 U.S.C. § 102(e) as being anticipated by Naven, U.S. Patent No. 5,936,956 ("Naven"). Claims 5, 14-19, and 23-28 were rejected under 35 U.S.C. § 103(a) as being unpatentable over Naven. A copy of claims 1, 3-9, and 12-29 on appeal is included in the Appendix hereto.

## IV. STATUS OF AMENDMENTS

An amendment is filed herewith to change the dependency of claim 18 from claim 16 to claim 17, in order to provide antecedent basis for "said third node" in claim 18. Appellants believe that the original dependency for claim 18 on claim 16 is a typographical error, only discovered in preparing this appeal brief. Appellants respectfully request that the amendment be entered in the present application. Claim 18 as shown in the included appendix reflects entry of the amendment.

## V. SUMMARY OF THE INVENTION

A computer system (10) may include a plurality of nodes (12A-12B). The computer system employs virtual channels and allocates different resources to the virtual channels (e.g. control packet buffers (60A-60D, 220, 222) and data buffers (60E-60G, 220, 222)). The nodes communicate using packets (30, 32, 34, 36, 212, 214) including control packets (30, 32, 34, 212, 214) which sometimes specify corresponding data packets (36). Packets are grouped into the virtual channels. The packets within a virtual channel may share resources (and hence experience resource conflicts), but the packets within different virtual channels may not share resources. Since packets which may experience resource conflicts do not experience logical conflicts, and since packets which may experience logical conflicts do not experience resource conflicts, deadlock-free operation may be achieved (see, e.g., page 3, lines 11-19).

Each virtual channel may be assigned control packet buffers and data buffers. If a control packet which does not specify a data packet is received, no data buffer space is allocated. If a control packet which does specify a data packet is received, both control packet buffer space and data packet buffer space is allocated. Since control packets are often smaller than data packets and occur more frequently, more buffer entries may be

provided within the control packet buffers than within the data packet buffers in some embodiments (see, e.g., page 3, line 21-page 4, line 1).

## VI. ISSUES

A. Whether claims 1, 3-4, 6-10, 12-13, 20-22, and 29 are patentable under 35 U.S.C. § 102(e) over Naven.

B. Whether claims 14-18 and 23-27 are patentable under 35 U.S.C. § 103(a) over Naven.

## VII. GROUPING OF CLAIMS

For purposes of the issues set forth in Section VI of this Appeal Brief only, the claims may be grouped as follows:

Claims 1 and 5 stand or fall together.

Claim 3 stands or falls alone.

Claim 4 stands or falls alone.

Claim 6 stands or falls alone.

Claim 7 stands or falls alone.

Claim 8 stands or falls alone.

Claims 9 and 19 stand or fall together.

Claim 12 stands or falls alone.

Claim 13 stands or falls alone.

Claim 14 stands or falls alone.

Claim 15 stands or falls alone.

Claim 16 stands or falls alone.

Claim 17 stands or falls alone.

Claim 18 stands or falls alone.

Claim 20 stands or falls alone.

Claim 21 stands or falls alone.

Claims 22 and 28 stand or fall together.

Claim 23 stands or falls alone.

Claim 24 stands or falls alone.

Claim 25 stands or falls alone.

Claim 26 stands or falls alone.

Claim 27 stands or falls alone.

Claim 29 stands or falls alone.

However, Appellants submit that each claim is independently patentable.

## VIII. ARGUMENT

Appellants note that each argument presented for a given claim below applies not only to that claim, but also to each claim dependent from that claim, including those dependent claims for which additional arguments are presented.

A. Rejection of Claims 1, 3-4, 6-10, 12-13, 20-22, and 29 Under 35 U.S.C. § 102(e) over Naven

Claims 1 and 5

Appellants respectfully submit that each of claims 1 and 5 recite combinations of features not taught or suggested in Naven. For example, claim 1 recites a combination of features including:

> receiving a first control packet in a first node of said plurality of nodes, said first node comprising a plurality of control packet buffers, each of said plurality of control packet buffers assigned to a different one of a plurality of virtual channels;
> determining a first virtual channel of said plurality of virtual channels to which said first control packet belongs;
> storing said first control packet in a first control packet buffer of said plurality of control packet buffers, said first control packet buffer assigned to said first virtual channel;
> receiving a first data packet specified by said first control packet; and
> storing said first data packet in a first data buffer of a plurality of data buffers within said first node, each of said plurality of data buffers assigned to a different one of said plurality of

virtual channels which includes at least one control packet which specifies a corresponding data packet.

These features are not taught or suggested in Naven.

The Office Actions in the present application appear to allege that the above highlighted features are taught in Naven at col. 4, lines 29-54 (see, e.g., Office Action mailed March 28, 2002; page 3, first paragraph). Appellants respectfully disagree. In this section, Naven discusses control information and data items (the payload portions of ATM cells). Naven teaches "the data storage means preferably store, for each preselected virtual channel, control information *for use in storing the received data items* in the linked list for the channel concerned and/or for use *in retrieving those stored data items from the linked list* for transfer to the further apparatus. The channel [sic] information may include, for example: a write pointer, indicating the location in the memory means of the last data block in the linked list in which the data of a received ATM cell was stored, and a read pointer indicating the location in the memory means of the next data block in the linked list that is to be transferred to the further apparatus" (Naven, col. 4, lines 17-28). Thus, Naven's control information is generated by the apparatus for storing and retrieving data items received by the apparatus.

Naven goes on to teach a "channel map having entries corresponding respectively to the available virtual channels of the group. Each of the entries identifies one of a plurality of control information storage portions that is associated individually with the virtual channel concerned" (Naven, col. 4, lines 33-37). Thus, the control information storage portions store the control information which, as highlighted above, is control information generated locally by the apparatus for controlling the storage of received data items.

Naven appears to describe his control information in more detail in col. 6-col. 7 and Fig. 3. Specifically, Naven teaches that "in order to control the output channels, the terminal controller 4 has, for each channel, a so-called 'descriptor' which contains, inter alia, information needed to store data in the linked list in the first stage of the above-

mentioned two stage data transfer operation and to retrieve the stored data from the linked list in the second stage" (Naven, col. 6, lines 61-66) and that "these descriptors are themselves stored in the local memory 5" (Naven, col. 7, lines 1-2). In col. 7, lines 7-30, Naven describes fields in the descriptor, including: (i) a Write Frame Start, Write Last Cell, Write Cell Count, Write Byte Count, and Write Status fields for adding a newly-received cell payload to the linked list; and (ii) a Read First Cell, Read Frame End, Read Cell Count, Read Byte Count, and Read Status fields used when reading the content of a stored data frame from the linked list for transfer to the main memory.

In view of the above, Naven's control information and received data items do not teach or suggest: "receiving a first control packet in a first node of said plurality of nodes, said first node comprising a plurality of control packet buffers, each of said plurality of control packet buffers assigned to a different one of a plurality of virtual channels; determining a first virtual channel of said plurality of virtual channels to which said first control packet belongs; storing said first control packet in a first control packet buffer of said plurality of control packet buffers, said first control packet buffer assigned to said first virtual channel" as recited in claim 1.

The Office Actions also refer to the abstract, col. 1, lines 21-39, col. 2, lines 1-29, and claim 1 of Naven in the rejection of claim 1. Appellants respectfully submit than none of these sections teach or suggest the above highlighted features of claim 1, either. For example, the abstract describes "receiving data from an ATM network, [and] a data storage circuit 38 for allocating preselected virtual channels of the network with respect to corresponding storage regions (5r) in a local memory (5)" (Naven, abstract, lines 1-4). "The data storage circuit 38 stores those [data items belonging to different preselected virtual channels] in the storage regions that correspond respectively to the items' virtual channels" (Naven, abstract, lines 6-10). The transfer of data items from the local memory 5 to other apparatus 7 may thus be performed in a different channel order than the order of receipt (Naven, abstract, lines 10-15). Thus, the abstract merely describes the receipt of data items, the storage of data items by virtual channel, and the forwarding of the data items to other apparatus in a different order. There is no discussion of control packets

and data packets in Naven's abstract, nor of a plurality of control packet buffers and a plurality of data buffers.

At col. 1, lines 21-29, Naven describes ATM cells as including 48 bytes of data and a 5 byte header that includes control information. However, Naven does not describe storing the header information in one set of buffers and the data payload in another set of buffers. While the data payload is stored in the local memory 5, the header information is not described as being stored. Instead, Naven teaches "The header portion HEAD is supplied to the address detection circuit 34, whilst the payload portion PAYL is supplied to the data storage circuit 38. The address detection circuit 34 takes the VPI/VCI fields of the header portion HEAD and forms a pointer address PADD by concatenating the least significant P bits of the VPI field and the least significant C bits of the VCI field. The pointer address PADD is supplied to the address translation circuit 36 which uses the pointer address to read, from the pointer storage region 5p, the pointer for the virtual channel to which the cell belongs" (Naven, col. 11, lines 45-56). Thus, the header portion is processed to find a pointer to store the data, but apparently is not stored in a set of buffers by virtual channel. These teachings do not teach or suggest the above highlighted features of claim 1.

At col. 1, lines 30-39, Naven describes the virtual paths and virtual channels defined for the ATM networks, and the VCI and VPI fields in the header to identify the virtual channel and virtual path. Nothing in this section teaches or suggests the above highlighted features of claim 1.

Similar to the abstract, Naven's col. 2, lines 1-29 describes a data receiving device for receiving ATM data, a data storage means for storing data on a virtual channel basis, and transferring the data out in a different channel order than received. Additionally, col. 2, lines 1-29 further describes high priority and low priority channels for data items. Still further, col. 2, lines 1-29 describes a receive queue that adds an entry for a virtual channel after one or more data items are stored to that virtual channel, for transferring data to another apparatus. Again, this discussion is focused on the handling of data items.

There is no discussion of control packets and data packets, nor of control packet buffers and data buffers. Naven's claim 1 describes an apparatus similar to the discussion of col. 2, lines 1-29 and does not appear to include any additional teachings over col. 2, lines 1-29.

Naven teaches storing data items in data buffers, controlled by locally-generated control information. Naven processes the headers of ATM cells to locate buffers to store the data items, but does not store the headers. None of these teachings from Naven teach or suggest:

> receiving a first control packet in a first node of said plurality of nodes, said first node comprising a plurality of control packet buffers, each of said plurality of control packet buffers assigned to a different one of a plurality of virtual channels;
> determining a first virtual channel of said plurality of virtual channels to which said first control packet belongs;
> storing said first control packet in a first control packet buffer of said plurality of control packet buffers, said first control packet buffer assigned to said first virtual channel;
> receiving a first data packet specified by said first control packet; and
> storing said first data packet in a first data buffer of a plurality of data buffers within said first node, each of said plurality of data buffers assigned to a different one of said plurality of virtual channels which includes at least one control packet which specifies a corresponding data packet.

as recited in claim 1.

Accordingly, Appellants respectfully submit that claim 1 is patentable over Naven for at least the above stated reasons. Claim 5, being dependent from claim 1, is similarly patentable over Naven for at least the above stated reasons. For at least all of the above stated reasons, Appellants respectfully submit that the rejection of claims 1 and 5 over Naven is in error and request reversal of the rejection.

Claim 3

Claim 3 is patentable over Naven for at least the reasons given above in support of claim 1. Additionally, claim 3 recites: "receiving a second control packet in said first node; determining a second virtual channel of said plurality of virtual channels to which said second control packet belongs, said second virtual channel being different from said first virtual channel; and storing said second control packet in a second control packet buffer of said plurality of control packet buffers, said second control packet buffer assigned to said second virtual channel." As highlighted above, Naven does not teach or suggest control packet buffers. Therefore, Naven cannot teach or suggest the above highlighted features of claim 3, either. The Office Actions' further discussion (with regard to claim 3) that Naven teaches routing packets among a plurality of nodes also do not teach or suggest the above highlighted features of claim 3.

For at least all of the above stated reasons, Appellants respectfully submit that the rejection of claim 3 over Naven is in error and request reversal of the rejection.

Claim 4

Claim 4 is patentable over Naven for at least the reasons given above in support of claims 1 and 3. Additionally, claim 4 recites: "transmitting said first control packet to a third node of said plurality of nodes, said third node comprising a second plurality of control packet buffers, each of said second plurality of control packet buffers assigned to a different one of said plurality of virtual channels, said transmitting responsive to a third control packet buffer of said second plurality of control packet buffers including space to store said first control packet, said third control packet buffer assigned to said first virtual channel; and transmitting said second control packet to said third node responsive to a fourth control packet buffer of said second plurality of control packet buffers including space to store said second control packet, said fourth control packet buffer assigned to said second virtual channel". The Office Action alleges that Naven implicitly discloses routing packets among a plurality of nodes. However, Naven does not teach or suggest "transmitting said first control packet to a third node ... responsive to a third control packet buffer of said second plurality of control packet buffers including space to store

said first control packet". Furthermore, Naven does not teach or suggest "transmitting said second control packet to said third node responsive to a fourth control packet buffer of said second plurality of control packet buffers including space to store said second control packet" as recited in claim 4.

For at least all of the above stated reasons, Appellants respectfully submit that the rejection of claim 4 over Naven is in error and request reversal of the rejection.

Claim 6

Claim 6 is patentable over Naven for at least the reasons given above in support of claim 1. Additionally, claim 6 recites: "determining that said first control packet belongs to a non-posted command virtual channel". The Office Action alleges that "Naven discloses determining a particular virtual channel to which a particular packet or control information belongs...therefore, Naven at least implicitly discloses the limitations of the claims 6-8 since the reference does limit the virtual channels any particular types" (see, e.g., Final Office Action mailed August 8, 2002; page 5, second paragraph). Appellants respectfully disagree. For a reference to anticipate a claim, the reference must teach each and every feature of the claim. Naven does not implicitly disclose the non-posted virtual channel. The lack of limitation of Naven to any particular type does not make the teachings of a specific type implicit. Furthermore, Naven explicitly discloses the ATM virtual channels (see, e.g., col. 1, lines 29-39), which are merely virtual channels identified by a number. Naven does not teach or suggest any other type of virtual channel. Thus, Naven does not teach or suggest a non-posted command virtual channel.

For at least all of the above stated reasons, Appellants respectfully submit that the rejection of claim 6 over Naven is in error and request reversal of the rejection.

Claim 7

Claim 7 is patentable over Naven for at least the reasons given above in support of claim 1. Additionally, claim 7 recites: "determining that said first control packet

belongs to a probe virtual channel". Naven does not implicitly disclose the probe virtual channel. The lack of limitation of Naven to any particular type does not make the teachings of a specific type implicit. Furthermore, Naven explicitly discloses the ATM virtual channels (see, e.g., col. 1, lines 29-39), which are merely virtual channels identified by a number. Naven does not teach or suggest any other type of virtual channel. Thus, Naven does not teach or suggest a probe virtual channel.

For at least all of the above stated reasons, Appellants respectfully submit that the rejection of claim 7 over Naven is in error and request reversal of the rejection.

Claim 8

Claim 8 is patentable over Naven for at least the reasons given above in support of claim 1. Additionally, claim 8 recites: " determining that said first control packet belongs to a response virtual channel." Naven does not implicitly disclose the response virtual channel. The lack of limitation of Naven to any particular type does not make the teachings of a specific type implicit. Furthermore, Naven explicitly discloses the ATM virtual channels (see, e.g., col. 1, lines 29-39), which are merely virtual channels identified by a number. Naven does not teach or suggest any other type of virtual channel. Thus, Naven does not teach or suggest a response virtual channel.

For at least all of the above stated reasons, Appellants respectfully submit that the rejection of claim 8 over Naven is in error and request reversal of the rejection.

Claim 20

Claim 20 is patentable over Naven for at least the reasons given above in support of claim 1. Additionally, claim 20 recites "each control packet included in at least one virtual channel of said plurality of virtual channels does not specify a data packet, and wherein none of said plurality of data buffers is assigned to said at least one virtual channel". These features do not appear to be treated in the Office Actions. Naven teaches ATM packets, which have a fixed size including 48 bytes of data and 5 bytes of header (Naven, col. 1, lines 24-29). Thus, Naven does not teach or suggest "each control

packet included in at least one virtual channel of said plurality of virtual channels does not specify a data packet" since all ATM packets have data. Furthermore, Naven does not teach or suggest "none of said plurality of data buffers is assigned to said at least one virtual channel".

For at least all of the above stated reasons, Appellants respectfully submit that the rejection of claim 20 over Naven is in error and request reversal of the rejection.

Claims 9 and 19

Appellants respectfully submit that each of claims 9 and 19 recites a combination of features not taught or suggested in Naven. For example, claim 9 recites a combination of features including:

> a first node configured to transmit a first control packet; and
> a second node coupled to receive said first control packet from said first node, wherein said second node comprises a plurality of control packet buffers, and wherein each of said plurality of control packet buffers is assigned to a different one of a plurality of virtual channels, and wherein said second node is configured to store said first control packet in a first control packet buffer of said plurality of control packet buffers responsive to a first virtual channel of said plurality of virtual channels to which said first control packet belongs, and wherein said second node further comprises a plurality of data buffers, each of said plurality of data buffers assigned to a different one of said plurality of virtual channels which includes at least one control packet which specifies a corresponding data packet, and wherein said first node is configured to transmit a first data packet specified by said first control packet, and wherein said second node is configured to store said first data packet in a first data buffer of said plurality of data buffers, said first data buffer assigned to said first virtual channel.

As highlighted above with regard to claim 1, Naven teaches storing data items in data buffers, controlled by locally-generated control information. Naven processes the headers of ATM cells to locate buffers to store the data items, but does not store the

headers. Thus, Naven cannot teach or suggest a plurality of control packet buffers and a plurality of data packet buffers, as recited in claim 9.

Accordingly, Appellants respectfully submit that claim 9 is patentable over Naven for at least the above stated reasons. Claim 19 being dependent from claim 9, are similarly patentable over Naven for at least the above stated reasons. For at least all of the above stated reasons, Appellants respectfully submit that the rejection of claims 9 and 19 over Naven is in error and request reversal of the rejection.

Claim 12

Claim 12 is patentable over Naven for at least the reasons given above in support of claim 9. Additionally, claim 12 recites: "said first node is configured to transmit a second control packet belonging to a second virtual channel of said plurality of virtual channels, said second virtual channel being different than said first virtual channel, and wherein said second node is configured to store said second control packet in a second control packet buffer of said plurality of control packet buffers". As highlighted above with regard to claim 9, Naven does not teach or suggest control packet buffers. Therefore, Naven cannot teach or suggest the above highlighted features of claim 12, either. The Office Actions' further discussion (with regard to claim 12) that Naven teaches routing packets among a plurality of nodes also do not teach or suggest the above highlighted features of claim 12.

For at least all of the above stated reasons, Appellants respectfully submit that the rejection of claim 12 over Naven is in error and request reversal of the rejection.

Claim 13

Claim 13 is patentable over Naven for at least the reasons given above in support of claims 9 and 12. Additionally, claim 13 recites: "wherein said second node is configured to transmit said first control packet to said third node *responsive to a third control packet buffer* of said second plurality of control packet buffers *including space to store said first control packet*, said third control packet buffer assigned to said first virtual

channel, and wherein said second node is configured to transmit said second control packet to said third node responsive to a fourth control packet buffer of said second plurality of control packet buffers including space to store said second control packet, said fourth control packet buffer assigned to said first virtual channel". The Office Action alleges that Naven implicitly discloses routing packets among a plurality of nodes. However, Naven does not teach or suggest "said second node is configured to transmit said first control packet to said third node *responsive to a third control packet buffer* of said second plurality of control packet buffers *including space to store said first control packet*", nor "transmit said second control packet to said third node responsive to a fourth control packet buffer of said second plurality of control packet buffers including space to store said second control packet", as recited in claim 13.

For at least all of the above stated reasons, Appellants respectfully submit that the rejection of claim 13 over Naven is in error and request reversal of the rejection.

Claim 21

Claim 21 is patentable over Naven for at least the reasons given above in support of claim 9. Additionally, claim 21 recites: "each control packet included in at least one virtual channel of said plurality of virtual channels does not specify a data packet, and wherein none of said plurality of data buffers is assigned to said at least one virtual channel". These features do not appear to be treated in the Office Actions. Naven teaches ATM packets, which have a fixed size including 48 bytes of data and 5 bytes of header (Naven, col. 1, lines 24-29). Thus, Naven does not teach or suggest "each control packet included in at least one virtual channel of said plurality of virtual channels does not specify a data packet" since all ATM packets have data. Furthermore, Naven does not teach or suggest "none of said plurality of data buffers is assigned to said at least one virtual channel".

For at least all of the above stated reasons, Appellants respectfully submit that the rejection of claim 21 over Naven is in error and request reversal of the rejection.

Claims 22 and 28

Appellants respectfully submit that each of claims 22 and 28 recites a combination of features not taught or suggested in Naven. For example, claim 22 recites a combination of features including:

> a plurality of control packet buffers, wherein each of said plurality of control packet buffers is assigned to a different one of a plurality of virtual channels;
> a plurality of data buffers, each of said plurality of data buffers assigned to a different one of said plurality of virtual channels which includes at least one control packet which specifies a corresponding data packet; and
> circuitry configured to store said first control packet in a first control packet buffer of said plurality of control packet buffers responsive to a first virtual channel of said plurality of virtual channels to which said first control packet belongs, and further configured to store said first data packet in a first data buffer of said plurality of data buffers, said first data buffer assigned to said first virtual channel.

As highlighted above with regard to claim 1, Naven teaches storing data items in data buffers, controlled by locally-generated control information. Naven processes the headers of ATM cells to locate buffers to store the data items, but does not store the headers. Thus, Naven cannot teach or suggest a plurality of control packet buffers and a plurality of data packet buffers, as recited in claim 22.

Accordingly, Appellants respectfully submit that claim 22 is patentable over Naven for at least the above stated reasons. Claim 28, being dependent from claim 22, is similarly patentable over Naven for at least the above stated reasons. For at least all of the above stated reasons, Appellants respectfully submit that the rejection of claims 22 and 28 over Naven is in error and request reversal of the rejection.

Claim 29

Claim 29 is patentable over Naven for at least the reasons given above in support of claim 22. Additionally, claim 29 recites: "each control packet included in at least one virtual channel of said plurality of virtual channels does not specify a data packet, and

wherein none of said plurality of data buffers is assigned to said at least one virtual channel". These features do not appear to be treated in the Office Action. Naven teaches ATM packets, which have a fixed size including 48 bytes of data and 5 bytes of header (Naven, col. 1, lines 24-29). Thus, Naven does not teach or suggest "each control packet included in at least one virtual channel of said plurality of virtual channels does not specify a data packet" since all ATM packets have data. Furthermore, Naven does not teach or suggest "none of said plurality of data buffers is assigned to said at least one virtual channel".

For at least all of the above stated reasons, Appellants respectfully submit that the rejection of claim 29 over Naven is in error and request reversal of the rejection.

B Rejection of Claims 14-18 and 23-27 Under 35 U.S.C. § 103(a) over Naven

Claim 14

Claim 14 is patentable over Naven for at least the reasons given above in support of claim 9. Additionally, claim 14 recites: "if said second node is a destination of said first control packet, said second node is configured to remove said first control packet from said first control packet buffer and to respond to said first control packet". As highlighted above with regard to claim 1, Naven does not teach or suggest control packet buffers. Accordingly, Naven cannot teach or suggest: "said second node is configured to remove said first control packet *from said first control packet buffer* and to respond to said first control packet". The Office Action alleges that moving control and data packets from their respective buffers may be considered implicit in Naven's teachings (see, e.g., Final Office Action, page 6, third paragraph). However, since Naven does not teach control packet buffers and data packet buffers, the above features of claim 14 are not implicit in Naven's teachings.

For at least all of the above stated reasons, Appellants respectfully submit that the rejection of claim 14 over Naven is in error and request reversal of the rejection.

Claim 15

Claim 15 is patentable over Naven for at least the reasons given above in support of claims 9 and 14. Furthermore, claim 15 recites "said second node is further configured to remove said first data packet from said first data buffer and to process said first data packet". These features, in combination with the features recited in claims 9 and 14, are not taught or suggested in Naven.

For at least all of the above stated reasons, Appellants respectfully submit that the rejection of claim 15 over Naven is in error and request reversal of the rejection.

Claim 16

Claim 16 is patentable over Naven for at least the reasons given above in support of claims 9, 14, and 15. Additionally, claim 16 recites: " said second node includes a cache and a memory controller, and wherein said second node is configured to provide said first data packet to one of said cache and said memory controller responsive to said first control packet". The Office Action alleges that the concept and advantage for a processor to send a command to a main storage device to request data to be cached in its local memory are well known. Irrespective of the correctness of this assertion, Appellant submits that this statement still does not teach or suggest "said second node is configured to provide said first data packet to *one of* said cache and said memory controller *responsive to said first control packet*". Even if Naven's system were modified to include a cache and a memory controller, it would not be obvious to provide a data packet to one or the other responsive to a control packet.

For at least all of the above stated reasons, Appellants respectfully submit that the rejection of claims 16 over Naven is in error and request reversal of the rejection.

Claim 17

Claim 17 is patentable over Naven for at least the reasons given above in support of claim 9. Additionally, claim 17 recites: "if said second node is not a destination of said first control packet, said second node is configured to remove said first control

packet from said first control packet buffer and to forward said first control packet to said third node". The Office Action alleges that these features are implicit in Naven's teachings. However, as highlighted above with regard to claim 9, Naven does not teach or suggest control packet buffers. Thus, "if said second node is not a destination of said first control packet, said second node is configured to remove said first control packet from said first control packet buffer and to forward said first control packet to said third node" cannot be implicit in Naven's teachings.

For at least all of the above stated reasons, Appellants respectfully submit that the rejection of claim 17 over Naven is in error and request reversal of the rejection.

Claim 18

Claim 18 is patentable over Naven for at least the reasons given above in support of claims 9 and 17. Furthermore, claim 18 recites "said second node is further configured to remove said first data packet from said first data buffer and to forward said first data packet to said third node". These features, in combination with the features recited in claims 9 and 17, are not taught or suggested in Naven.

For at least all of the above stated reasons, Appellants respectfully submit that the rejection of claim 18 over Naven is in error and request reversal of the rejection.

Claim 23

Claim 23 is patentable over Naven for at least the reasons given above with regard to claim 22. Additionally, claim 23 recites: " if said node is a destination of said first control packet, said circuitry is configured to remove said first control packet from said first control packet buffer, and wherein said node is configured to respond to said first control packet". The Office Action alleges that removing control and data packets from their respective buffers may be considered implicit in Naven's teachings. However, since Naven does not teach control packet buffers and data packet buffers, the above features of claim 23 are not implicit in Naven's teachings.

For at least all of the above stated reasons, Appellants respectfully submit that the rejection of claim 23 over Naven is in error and request reversal of the rejection.

Claim 24

Claim 24 is patentable over Naven for at least the reasons given above in support of claims 22 and 23. Furthermore, claim 24 recites "said circuitry is further configured to remove said first data packet from said first data buffer and, wherein said node is configured to process said first data packet". These features, in combination with the features recited in claims 22 and 23, are not taught or suggested in Naven.

For at least all of the above stated reasons, Appellants respectfully submit that the rejection of claim 24 over Naven is in error and request reversal of the rejection.

Claim 25

Claim 25 is patentable over Naven for at least the reasons given above with regard to claims 22, 23, and 24. Additionally, claim 25 recites: "a cache and a memory controller, and wherein said node is configured to provide said first data packet to one of said cache and said memory controller responsive to said first control packet." The Office Action alleges that the concept and advantage for a processor to send a command to a main storage device to request data to be cached in its local memory are well known. Irrespective of the correctness of this assertion, Appellant submits that this statement still does not teach or suggest "said node is configured to provide said first data packet to *one of* said cache and said memory controller *responsive to said first control packet*". Even if Naven's system were modified to include a cache and a memory controller, it would not be obvious to provide a data packet to one or the other responsive to a control packet.

For at least all of the above stated reasons, Appellants respectfully submit that the rejection of claim 25 over Naven is in error and request reversal of the rejection.

Claim 26

Claim 26 is patentable over Naven for at least the reasons given above in support

of claim 22. Additionally, claim 26 recites: "if said second node is not a destination of said first control packet, said circuitry is configured to remove said first control packet from said first control packet buffer and to forward said first control packet to another node." The Office Action alleges that these features are implicit in Naven's teachings. However, as highlighted above with regard to claim 22, Naven does not teach or suggest control packet buffers. Thus, "if said second node is not a destination of said first control packet, said circuitry is configured to remove said first control packet from said first control packet buffer and to forward said first control packet to another node" cannot be implicit in Naven's teachings.

For at least all of the above stated reasons, Appellants respectfully submit that the rejection of claim 26 over Naven is in error and request reversal of the rejection.

Claim 27

Claim 27 is patentable over Naven for at least the reasons given above in support of claims 22 and 26. Furthermore, claim 27 recites "said circuitry is further configured to remove said first data packet from said first data buffer and to forward said first data packet to said another node". These features, in combination with the features recited in claims 22 and 26, are not taught or suggested in Naven.

For at least all of the above stated reasons, Appellants respectfully submit that the rejection of claim 27 over Naven is in error and request reversal of the rejection.

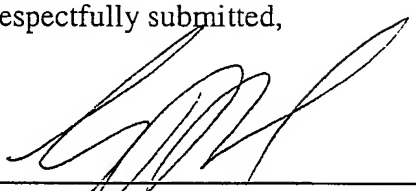
## IX. CONCLUSION

For at least the foregoing reasons, Appellants respectfully submit that the Examiner's rejections of claims 1, 3-9, and 12-29 were erroneous and respectfully request the Board of Patent Appeals to reverse the Examiner's rejections.

A Fee Authorization Form authorizing a deposit account charge for the fee for filing an appeal brief under 37 C.F.R. § 1.17(c) is enclosed. If the fee is missing or insufficient, or if any other fees are due, the Commissioner is authorized to charge said

fees to Deposit Account No. 501505/5500-46300/LJM.

Respectfully submitted,



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Date: 12/18/02

## X. APPENDIX

This appendix includes a copy of the claims involved in this appeal.

1. A method for routing packets among a plurality of nodes in a computer system, the method comprising:

receiving a first control packet in a first node of said plurality of nodes, said first node comprising a plurality of control packet buffers, each of said plurality of control packet buffers assigned to a different one of a plurality of virtual channels;

determining a first virtual channel of said plurality of virtual channels to which said first control packet belongs;

storing said first control packet in a first control packet buffer of said plurality of control packet buffers, said first control packet buffer assigned to said first virtual channel;

receiving a first data packet specified by said first control packet; and

storing said first data packet in a first data buffer of a plurality of data buffers within said first node, each of said plurality of data buffers assigned to a different one of said plurality of virtual channels which includes at least one control packet which specifies a corresponding data packet.

3. The method as recited in claim 1 further comprising:

receiving a second control packet in said first node;

determining a second virtual channel of said plurality of virtual channels to which said second control packet belongs, said second virtual channel being

different from said first virtual channel; and

storing said second control packet in a second control packet buffer of said plurality of control packet buffers, said second control packet buffer assigned to said second virtual channel.

4. The method as recited in claim 3 further comprising:

transmitting said first control packet to a third node of said plurality of nodes, said third node comprising a second plurality of control packet buffers, each of said second plurality of control packet buffers assigned to a different one of said plurality of virtual channels, said transmitting responsive to a third control packet buffer of said second plurality of control packet buffers including space to store said first control packet, said third control packet buffer assigned to said first virtual channel; and

transmitting said second control packet to said third node responsive to a fourth control packet buffer of said second plurality of control packet buffers including space to store said second control packet, said fourth control packet buffer assigned to said second virtual channel.

5. The method as recited in claim 1 wherein said determining comprises decoding a command field of said first control packet.

6. The method as recited in claim 1 wherein said determining comprises determining that said first control packet belongs to a non-posted command virtual channel.

7. The method as recited in claim 1 wherein said determining comprises determining that said first control packet belongs to a probe virtual channel.

8. The method as recited in claim 1 wherein said determining comprises determining that

said first control packet belongs to a response virtual channel.

9. A computer system comprising:

a first node configured to transmit a first control packet; and

a second node coupled to receive said first control packet from said first node, wherein said second node comprises a plurality of control packet buffers, and wherein each of said plurality of control packet buffers is assigned to a different one of a plurality of virtual channels, and wherein said second node is configured to store said first control packet in a first control packet buffer of said plurality of control packet buffers responsive to a first virtual channel of said plurality of virtual channels to which said first control packet belongs, and wherein said second node further comprises a plurality of data buffers, each of said plurality of data buffers assigned to a different one of said plurality of virtual channels which includes at least one control packet which specifies a corresponding data packet, and wherein said first node is configured to transmit a first data packet specified by said first control packet, and wherein said second node is configured to store said first data packet in a first data buffer of said plurality of data buffers, said first data buffer assigned to said first virtual channel.

12. The computer system as recited in claim 9 wherein said first node is configured to transmit a second control packet belonging to a second virtual channel of said plurality of virtual channels, said second virtual channel being different than said first virtual channel, and wherein said second node is configured to store said second control packet in a second control packet buffer of said plurality of control packet buffers.

13. The computer system as recited in claim 12 wherein said further comprising a third node including a second plurality of control packet buffers, each of said second plurality

of control packet buffers assigned to a different one of said plurality of virtual channels, wherein said second node is configured to transmit said first control packet to said third node responsive to a third control packet buffer of said second plurality of control packet buffers including space to store said first control packet, said third control packet buffer assigned to said first virtual channel, and wherein said second node is configured to transmit said second control packet to said third node responsive to a fourth control packet buffer of said second plurality of control packet buffers including space to store said second control packet, said fourth control packet buffer assigned to said first virtual channel.

14. The computer system as recited in claim 9 wherein, if said second node is a destination of said first control packet, said second node is configured to remove said first control packet from said first control packet buffer and to respond to said first control packet.

15. The computer system as recited in claim 14 wherein said second node is further configured to remove said first data packet from said first data buffer and to process said first data packet.

16. The computer system as recited in claim 15 wherein said second node includes a cache and a memory controller, and wherein said second node is configured to provide said first data packet to one of said cache and said memory controller responsive to said first control packet.

17. The computer system as recited in claim 9 further comprising a third node coupled to receive packets from said second node, wherein, if said second node is not a destination of said first control packet, said second node is configured to remove said first control packet from said first control packet buffer and to forward said first control packet to said third node.

18. The computer system as recited in claim 17 wherein said second node is further

configured to remove said first data packet from said first data buffer and to forward said first data packet to said third node.

19. The computer system as recited in claim 9 wherein said second node is configured to determine said first virtual channel to which said first control packet belongs by decoding a command field of said first control packet.

20. The method as recited in claim 1 wherein each control packet included in at least one virtual channel of said plurality of virtual channels does not specify a data packet, and wherein none of said plurality of data buffers is assigned to said at least one virtual channel.

21. The computer system as recited in claim 9 wherein each control packet included in at least one virtual channel of said plurality of virtual channels does not specify a data packet, and wherein none of said plurality of data buffers is assigned to said at least one virtual channel.

22. A node coupled to receive a first control packet and a first data packet specified by said first control packet, the node comprising:

a plurality of control packet buffers, wherein each of said plurality of control packet buffers is assigned to a different one of a plurality of virtual channels;

a plurality of data buffers, each of said plurality of data buffers assigned to a different one of said plurality of virtual channels which includes at least one control packet which specifies a corresponding data packet; and

circuitry configured to store said first control packet in a first control packet buffer of said plurality of control packet buffers responsive to a first virtual channel of said plurality of virtual channels to which said first

control packet belongs, and further configured to store said first data packet in a first data buffer of said plurality of data buffers, said first data buffer assigned to said first virtual channel.

23. The node as recited in claim 22 wherein, if said node is a destination of said first control packet, said circuitry is configured to remove said first control packet from said first control packet buffer, and wherein said node is configured to respond to said first control packet.

24. The node as recited in claim 23 wherein said circuitry is further configured to remove said first data packet from said first data buffer and, wherein said node is configured to process said first data packet.

25. The node as recited in claim 24 further comprising a cache and a memory controller, and wherein said node is configured to provide said first data packet to one of said cache and said memory controller responsive to said first control packet.

26. The node as recited in claim 22 wherein, if said second node is not a destination of said first control packet, said circuitry is configured to remove said first control packet from said first control packet buffer and to forward said first control packet to another node.

27. The node as recited in claim 26 wherein said circuitry is further configured to remove said first data packet from said first data buffer and to forward said first data packet to said another node.

28. The node as recited in claim 22 wherein said circuitry is configured to determine said first virtual channel to which said first control packet belongs by decoding a command field of said first control packet.

29. The node as recited in claim 22 wherein each control packet included in at least one

virtual channel of said plurality of virtual channels does not specify a data packet, and wherein none of said plurality of data buffers is assigned to said at least one virtual channel.

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Inventor(s): Keller et al.
Assignee: Advanced Micro Devices, Inc.
Serial No.: 09/399,281
Filing Date: 9/17/99
Title: VIRTUAL CHANNELS AND CORRESPONDING BUFFER ALLOCATIONS FOR DEADLOCK-FREE COMPUTER SYSTEM OPERATION
Atty. Docket No. 5500-46300; TT3324



The date stamp of the mail room of the U.S. Patent and Trademark Office hereon will acknowledge receipt of the attached 1) Petition under 37 C.F.R. § 1.181(a); 2) Practitioner's Statement; 3) Copy of previously submitted Appeal Brief mailed December 18, 2002, Amendment, Marked-up Copy of Amended Claims, Fee Authorization form and return receipt postcard; and 4) Return Postcard.

LJM\dmp Via First Class Mail Date: May 29, 2003